

1 ~~151~~. (Amended) A synchronous integrated circuit device having
2 a memory array which includes dynamic random access memory cells,
3 wherein the integrated circuit device comprises:
4 a clock receiver to receive an external clock signal;
5 a plurality of sense amplifiers, coupled to the memory array,
6 to sense data from the dynamic random access memory cells; and
7 a plurality of input receivers to sample an operation code
8 synchronously with respect to the external clock signal, the
9 operation code including precharge information, wherein, in
10 response to the precharge information, the plurality of sense
11 amplifiers is automatically precharged after the data is sensed.

1 ~~152~~. The integrated circuit device of claim ~~151~~ wherein the
2 operation code specifies a read operation, and wherein the
3 integrated circuit device further includes a plurality of output
4 drivers to output first and second portions of the data in response
5 to the operation code specifying a read operation.

1 ~~153~~. The integrated circuit device of claim ~~152~~ wherein:
2 the plurality of output drivers output the first portion of
3 the data synchronously with respect to a rising edge transition of
4 the external clock signal; and
5 the plurality of output drivers output a second portion of the
6 data synchronously with respect to a falling edge transition of the
7 external clock signal.

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1 ~~154~~. (Amended) The integrated circuit device of claim ~~152~~ 2
2 further including a delay lock loop, coupled to the plurality of
3 output drivers, to synchronize the output of the first and second
4 portions of the data with the external clock signal.

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1 ~~155~~. (Amended) The integrated circuit device of claim ~~152~~ 2
2 further including a plurality of multiplexers to provide the first
3 and second portions of data to the plurality of output drivers,
4 wherein each multiplexer of the plurality of multiplexers is
5 coupled to a respective output driver of the plurality of output
6 drivers.

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1 ~~156~~. The integrated circuit device of claim ~~155~~ 5 wherein:
2 the plurality of multiplexers provide the first portion of the
3 data to the plurality of output drivers in response to a rising
4 transition of the external clock signal; and
5 the plurality of multiplexers provide the second portion of
6 the data to the plurality of output drivers in response to a
7 falling edge transition of the external clock signal.

1 ⁷~~157~~. (Amended) The integrated circuit device of claim ¹~~151~~
2 wherein the plurality of input receivers further includes a first
3 input receiver to sample a first bit of the operation code
4 synchronously with respect to the external clock signal, wherein
5 the precharge information is encoded in the first bit of the
6 operation code.

B1 1 ⁸~~158~~. (Amended) The integrated circuit device of claim ⁷~~157~~
2 wherein the plurality of input receivers further includes a second
3 input receiver to sample a second bit of the operation code
4 synchronously with respect to the external clock signal, wherein
5 the second bit of the operation code specifies a read operation,
6 wherein a portion of the data is output from the integrated circuit
7 device in response to the second bit of the operation code
8 specifying the read operation.

1 ⁹~~159~~. The integrated circuit device of claim ⁸~~158~~ wherein the
2 plurality of input receivers further includes a third input
3 receiver to sample address information synchronously with respect
4 to the external clock signal.

1 ¹⁰~~160~~. (Amended) The integrated circuit device of claim ¹~~151~~
2 wherein the operation code includes a plurality of bits that, in
3 combination, encode information which specifies that the plurality
4 of sense amplifiers sense the data from the memory array.

11
1 ~~161~~. The integrated circuit device of claim ~~151~~ further
2 including row decoder circuitry, coupled to the memory array, to
3 identify, in response to a row address, a row of the memory array
4 that stores the data to be sensed by the plurality of sense
5 amplifiers.

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1 ~~162~~. The integrated circuit device of claim ~~151~~ further
2 including column decoder circuitry, coupled to the plurality of
3 sense amplifiers, to identify, in response to a column address, a
4 portion of the data.

13
1 ~~163~~. The integrated circuit device of claim ~~151~~ further
2 including a clock synchronization circuit coupled to the clock
3 receiver, wherein the clock synchronization circuit includes:
4 a delay line to generate an internal clock signal, wherein the
5 internal clock signal has a delay with respect to the external
6 clock signal; and
7 a comparator to compare the internal clock signal with the
8 external clock signal, wherein the delay of the internal clock
9 signal is adjusted based on the comparison between the internal
10 clock signal and the external clock signal.

1 ¹⁴~~164~~. (Amended) The integrated circuit device of claim ¹³~~163~~
2 further including a plurality of output drivers to output first and
3 second portions of the data in response to the operation code
4 specifying a read operation, wherein the clock synchronization
5 circuit is coupled to the plurality of output drivers to
6 synchronize the output of the first and second portions of the data
7 with the external clock signal.

8 ¹⁵~~165~~. (Amended) The integrated circuit device of claim ¹⁴~~164~~
9 wherein the plurality of input receivers samples the operation code
10 from a plurality of external signal lines of an external bus,
11 wherein the external bus is used to carry, in a multiplexed format,
12 the operation code, and the first and second portions of the data.

¹⁶

1 ~~166~~. A synchronous integrated circuit memory device including
2 an array of memory cells, wherein the memory device comprises:
3 a clock receiver to receive an external clock signal;
4 a plurality of sense amplifiers, coupled to the array of
5 memory cells, to sense data, wherein a portion of the data is
6 output from the memory device in response to a first operation code
7 bit specifying a read operation;
8 a first input receiver to sample the first operation code bit
9 in response to a first transition of the external clock signal;
10 a second input receiver to sample a second operation code bit
11 in response to the first transition of the external clock signal,
12 wherein the second operation code bit indicates whether precharging
13 the plurality of sense amplifiers occurs automatically after the
14 data has been sensed; and
15 a plurality of output drivers to output the portion of the
16 data synchronously with respect to the external clock signal.

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1 ~~167~~. The memory device of claim ~~166~~ wherein the second input
2 receiver further samples an address bit synchronously with respect
3 to a second transition of the external clock signal.

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1 ~~168~~. The memory device of claim ~~166~~ wherein the plurality of
2 output drivers output the portion of the data onto an external bus,
3 the external bus including a plurality of external signal lines.

1 ¹⁹~~169~~. The memory device of claim ¹⁸~~168~~ wherein:
2 the first operation code bit is sampled from a first signal
3 line of the plurality of external signal lines; and
4 the second operation code bit is sampled from a second signal
5 line of the plurality of external signal lines.

1 ²⁰~~170~~. The memory device of claim ¹⁹~~169~~ wherein the plurality of
2 external signal lines is used to carry, in a multiplexed format,
3 address information and the portion of the data.

1 ²¹~~171~~. The memory device of claim ¹⁶~~166~~ further including a delay
2 locked loop, coupled to the clock receiver, to generate an internal
3 clock signal using the external clock signal, wherein the plurality
4 of output drivers output the portion of the data in response to the
5 internal clock signal.

1 ²²~~172~~. (Amended) The memory device of claim ¹⁶~~166~~ further
2 including:
3 row decoder circuitry, coupled to the array of memory cells,
4 to identify a row of the array of memory cells that stores the data
5 to be sensed by the plurality of sense amplifiers; and
6 column decoder circuitry, coupled to the plurality of sense
7 amplifiers, to identify the portion of the data.

²³
~~173~~. A method of operation of a synchronous integrated
circuit memory device, wherein the memory device includes an array
of memory cells, wherein the method of operation of the memory
device comprises:
sampling an operation code in response to a first transition
of an external clock signal, wherein the operation code specifies a
read operation and includes precharge information;
sensing data in a plurality of sense amplifiers, wherein the
data is output in response to the operation code specifying the
read operation;
automatically precharging the plurality of sense amplifiers in
response to the precharge information, wherein the plurality of
sense amplifiers is automatically precharged after the data is
sensed; and
outputting the data synchronously with respect to the external
clock signal.

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~~174~~. (Amended) The method of claim ²³~~173~~ further including
sampling address information synchronously with respect to the
external clock signal, wherein the address information identifies a
location of the data within the array.

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~~175~~. The method of claim ²⁴~~174~~ wherein the operation code and
the address information are included in a request packet.

1 ²⁶~~176~~. The method of claim ²⁴~~174~~ wherein the operation code and
2 the address information are sampled from an external bus, wherein
3 the external bus includes a plurality of signal lines to carry the
4 address information and the operation code in a multiplexed format.

1 ²⁷~~177~~. The method of claim ²⁶~~175~~ wherein the data is output onto
2 the plurality of signal lines.

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1 ²⁸~~178~~. The method of claim ²³~~173~~ further including:
2 selecting a row of memory cell locations in accordance with a
3 first address portion; and
4 sensing data, from the selected row of memory cell locations,
5 in a row of sense amplifiers, wherein the plurality of sense
6 amplifiers is included in the row of sense amplifiers.

1 ²⁹~~179~~. (Amended) The method of claim ²⁸~~178~~ further including
2 identifying the data sensed in the plurality of sense amplifiers
3 based on a second address portion.

1 ³⁰~~180~~. The method of claim ²³~~173~~ further including generating an
2 internal clock signal using a delay locked loop, wherein the data
3 is output in response to the internal clock signal.

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1 ³¹~~181~~. (Amended) The method of claim ²³~~173~~ wherein outputting the
2 data includes:

3 outputting a first portion of the data synchronously with
4 respect to a rising edge transition of the external clock signal;
5 and

B 6 outputting a second portion of the data synchronously with
7 respect to a falling edge transition of the external clock signal.

1 ³²~~182~~. A method of controlling a synchronous memory device,
2 wherein the memory device includes a plurality of sense amplifiers
3 coupled to a memory cell array, wherein the method of controlling
4 the memory device comprises:

5 providing a first operation code to the memory device, wherein
6 the first operation code indicates that the memory device:

7 output data read from the memory cell array; and

8 precharge sense amplifiers used in reading the data from
9 the memory cell array, wherein the sense amplifiers used in
10 reading the data are precharged automatically after the data
11 is read from the memory cell array; and

12 receiving the data from the memory device, the memory device
13 outputting the data in response to the first operation code.

1 ³³~~183~~. The method of claim ³²~~182~~ wherein the first operation code
2 is included in a request packet.

1 ³⁴~~184~~. (Amended) The method of claim ³²~~182~~ further including
2 providing a second operation code to the memory device, wherein the
3 second operation code instructs the memory device to:
4 receive input data to be written to the memory cell array;
5 write the input data to the memory cell array using sense
6 amplifiers of the plurality of sense amplifiers; and
7 precharge the sense amplifiers used in writing the input data
8 to the memory cell array, wherein the sense amplifiers are
9 precharged automatically after the input data is written to the
10 memory cell array.

1 ³⁵~~185~~. The method of claim ³⁴~~184~~ further including:
2 providing, to the memory device, a row address and a column
3 address; and
4 providing a third operation code to the memory device, wherein
5 the third operation code instructs the memory device to:
6 output data read from a specified location of the memory
7 cell array, wherein the specified location is identified by
8 the row address and the column address; and
9 retaining, in at least a portion of the plurality of
10 sense amplifiers, the data read from the specified location of
11 the memory cell array.

³⁶³²

~~186~~. (Amended) The method of claim ~~182~~ further including:

providing, to the memory device, a row address; and

providing a second operation code to the memory device,

wherein the second operation code includes bits that, in

combination, encode information which indicates that the memory

device sense data from a specified location of the memory cell

array using at least a portion of the plurality of sense

amplifiers, wherein the specified location is identified by the row

address.

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~~187~~. The method of claim ~~182~~ further including providing

address information to the memory device, wherein the address

information is provided synchronously with respect to the external

clock signal.

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~~188~~. The method of claim ~~187~~ wherein the address information

and the first operation code are issued to the memory device via an

external bus.

1 ³⁹~~189~~. (Amended) A synchronous memory device having a memory
2 array which includes dynamic memory cells, wherein the memory
3 device comprises:

4 a plurality of sense amplifiers, coupled to the memory array,
5 to sense data from the dynamic memory cells;

6 a plurality of input receivers to sample an operation code
7 synchronously with respect to an external clock signal, the
8 operation code including precharge information, wherein, in
9 response to the precharge information, the plurality of sense
10 amplifiers is automatically precharged after the data is sensed;

B 11 a plurality of output drivers to output first and second
12 portions of the data in response to the operation code specifying a
13 read operation; and

14 a delay locked loop, coupled to the plurality of output
15 drivers, to synchronize the output of the first and second portions
16 of the data with the external clock signal.

1 ⁴⁰~~190~~. The memory device of claim ³⁹~~189~~ wherein:

2 the plurality of output drivers output the first portion of
3 the data synchronously with respect to a rising edge transition of
4 the external clock signal; and

5 the plurality of output drivers output the second portion of
6 the data synchronously with respect to a falling edge transition of
7 the external clock signal.

1 ⁴¹~~191~~. (Amended) The memory device of claim ³⁹~~189~~ further
2 including a plurality of multiplexers, wherein each multiplexer of
3 the plurality of multiplexers is coupled to a respective output
4 driver of the plurality of output drivers.

1 ⁴²~~192~~. (Amended) The memory device of claim ⁴¹~~191~~ wherein the
2 plurality of multiplexers provides the first portion of the data to
3 the plurality of output drivers in response to a rising edge
4 transition of the external clock signal, and wherein the plurality
5 of multiplexers provides the second portion of the data to the
6 plurality of output drivers in response to a falling edge
7 transition of the external clock signal.

1 ⁴³~~193~~. (Amended) The memory device of claim ³⁹~~189~~ wherein the
2 plurality of input receivers further includes a first input
3 receiver to sample a first bit of the operation code synchronously
4 with respect to the external clock signal, wherein the precharge
5 information is encoded in the first bit of the operation code.

1 ⁴⁴~~194~~. (Amended) The memory device of claim ⁴³~~183~~ wherein the
2 plurality of input receivers further includes a second input
3 receiver to sample a second bit of the operation code synchronously
4 with respect to the external clock signal, wherein an encoding of
5 the second bit of the operation code specifies the read operation.

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1 ⁴⁵~~195~~. (Amended) The memory device of claim ³⁹~~189~~ wherein the
2 delay locked loop includes:
3 a delay line to generate an internal clock signal, wherein the
4 internal clock signal has a delay with respect to the external
5 clock signal; and
6 a comparator to compare the internal clock signal with the
7 external clock signal, wherein the delay of the internal clock
8 signal is adjusted based on the comparison between the internal
9 clock signal and the external clock signal, wherein the output of
10 the first and second portions of the data is synchronized with the
11 external clock signal using the internal clock signal.

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